

# High Performance, Low-Noise, 128-Channel Readout Integrated Circuit for Flat Panel X-ray Detector Systems

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## ABSTRACT

A silicon mixed-signal integrated circuit is needed to extract and process x-ray induced signals from a coated flat panel thin film transistor array (TFT) in order to generate a digital x-ray image. Indigo Systems Corporation has designed, fabricated, and tested such a readout integrated circuit (ROIC), the ISC9717. This off-the-shelf, high performance, low-noise, 128-channel device is fully programmable with a multistage pipelined architecture and a 9 to 14-bit programmable A/D converter per channel, making it suitable for numerous X-ray medical imaging applications. These include high-resolution radiography in single frame mode and fluoroscopy where high frame rates are required.

The ISC9717 can be used with various flat panel arrays and solid-state detectors materials: Selenium (Se), Cesium Iodide (CsI), Silicon (Si), Amorphous Silicon, Gallium Arsenide (GaAs), and Cadmium Zinc Telluride (CdZnTe). The 80-micron pitch ROIC is designed to interface (wire bonding or flip-chip) along one or two sides of the x-ray panel, where ROICs are abutted vertically, each reading out charge from pixels multiplexed onto 128 horizontal read lines.

The paper will present the design and test results of the ROIC, including the mechanical and electrical interface to a TFT array, system performance requirements, output multiplexing of the digital signals to an off-board processor, and characterization test results from fabricated arrays.

**Keywords:** ASIC, readout integrated circuit (ROIC), CMOS, thin film transistor (TFT), multiplexing, digital x-ray image, A/D converter, integration time, correlated double sampling, low-pass filter

## 1. INTRODUCTION

As digital imaging sensor technology advances, requirements have evolved for new and improved methods of acquiring and processing the detector output signals for generation of high quality imagery. Indigo's expertise in silicon mixed-signal integrated circuit technology provided a basis for design and fabrication of such devices. The ISC9717 readout integrated circuit was primarily developed to support x-ray flat panel arrays containing thousands of elements. The device also supports linear x-ray detector systems for industrial applications such as airport security scanning systems.

Requirements for an effective design were compiled and resulted in a readout circuit compatible with a range of detector array characteristics. The ISC9717 is a low-noise 128-channel device that is fully programmable for both input signal polarities (electrons and holes), pixel averaging, gain, low pass filter time constants, correlated double sampling and up to 14-bit A/D converter resolution. An 80-micron pitch was selected for the device with an interface designed for wire bonding or flip-chip bonding, depending on the constraints of the detector interface, pitch and system requirements.

The ISC9717 ROIC is novel in its design flexibility and digital output, compatible for use with various flat panel arrays and solid-state detectors materials (Selenium, Cesium Iodide, Silicon, Amorphous Silicon, Gallium Arsenide, and Cadmium Zinc Telluride). No other commercially available readout circuit operates over such a wide range of signal levels, supporting many x-ray applications. Table 1 shows examples for fluoroscopy (high frame rate output), radiography (high dynamic range snapshot) and mammography (high resolution snapshot). An example of compatible detector characteristics is shown on Table 2.

Application	ADC resolution	Dynamic Range	Frame Rate
Fluoroscopy	9 to 11 bits	$0.5 \times 10^6$ (80fC)	30 to 60 Hz (depending on array size)
Radiography	12 to 14 bits	$75 \times 10^6$ (12pC)	Snapshot
Mammography	12 to 14 bits	$10^6$ to $75 \times 10^6$ (12pC)	Snapshot

Table 1: Example of medical imaging applications supported by the ISC9717 (electron or hole collection)

Specifications	Nominal	Comments
Data line voltage	1.5 to 3.5V (virtual ground)	Integrator input DC operating point adjusted externally
Carrier collected	Electrons or Holes	
Photodiode capacitance	0.7 pF	
Data line capacitance	100 pF	20 cm of data line
Data line series resistance	1 k $\Omega$	
Signal time constant	2.8ms	$R_{ON} \times C_{\text{photodiode}}$ ( $R_{ON} = 4\text{Meg}\Omega$ )
Data Line to Data Line Capacitance	1pF	
Maximum signal dynamic range	14 bit	Signal/Noise
Clock feedthrough	0.4pC	Injection due to the TFT switch (TFTON is the opposite polarity of the signal)
Charge left after TFT ON/OFF	$\leq 2.9\text{fC}$	
Array size	3200x2304	Pixel size = $127 \times 127 \mu\text{m}^2$
Temperature of operation	10 to 60°C	

Table 2: Example of Compatible Detector Characteristics

## 2. DESIGN SPECIFICATIONS AND ARCHITECTURE

The ISC9717 was specified to meet requirements for flat panel x-ray systems as well as industrial instrumentation. The low noise characteristics, selectable gain, filtering, A/D resolution, charge carrier selection and other programmable features are explained in detail.

Parameters for the integrated circuit are specified in Table 3 and Table 4. Nominal values are given with comments and verification of performance per Indigo's characterization testing. The testing is outlined in section 5.

Specifications	Nominal	Comments
<b>Input DC offset (virtual ground)</b>	adjustable from 1.5V to 3.5V	The integrator DC operating point is adjusted for optimum dynamic range (hole or electron collection)
<b>Correlated Double Sampling</b>	Removes the ROIC kTC and 1/f noise	
<b>Crosstalk (internal to ROIC)</b>	$\leq \pm 0.25\%$	
<b>Number of channel</b>	128 channel/chip	
<b>Channel pitch</b>	80 $\mu\text{m}$	Input bonding pad pitch
<b>Number of interface pads</b>	39 pads	
<b>Chip size (length)</b>	$\approx 11.15\text{mm}$	39 pads x 280 $\mu\text{m} \approx 11\text{mm}$
<b>Chip size (width)</b>	$\approx 4.74\text{mm}$	
<b>Total power dissipation</b>	$\leq 220\text{mW}$	
<b>Integrator gain control</b>	$C_F = 0.5\text{pF}, 1\text{pF}, 2\text{pF}, 4\text{pF}$ (default = 0.5pF)	2BIT gain control
<b>Low-Pass-Filter Time constant</b>	0.8 $\mu\text{s}, 1.3\mu\text{s}, 2.8\mu\text{s}, 3.3\mu\text{s}$ ( $\pm 10\%$ tolerance)	2BIT (2 capacitors selectable) (default = 0.8 $\mu\text{s}$ )

Table 3. ISC9717 Specification and Performance (1 of 2)

Specifications	Nominal	Comments
<b>Clock frequency</b>	12.5MHz	Low voltage differential clock
<b>Input control signals (CLK, SYNC, DATA_IN)</b>	$\geq \pm 100\text{mV}$ differential $1\text{V} < \text{signal} < 3.5$ Rise / fall time $< 10\text{ns}$	Low voltage differential Common mode = [1, 3.5] Rise /fall time = 10% to 90%
<b>Programmable gain stage</b>	$\geq \times 1, \times 2, \times 4, \times 8, \times 32$	4 gain settings
<b>ADC resolution</b>	9 to 14 bits (gray code output)	Programmable ADC resolution
<b>ADC INL</b>	$< \pm 0.5\text{LSB}$	By design
<b>ADC clock</b>	25MHz	Twice the master clock rate
<b>Number of output</b>	14	Single ended, current mode output
<b>Output signal</b>	$0.5\text{mA} \pm 10\%$ across bits Absolute value $0.5\text{mA} \pm 20\%$	PMOS open drain current output Depends on receiver stage input impedance
<b>Readout rate</b>	12.5MHz	128 channel @ 12.5MHz = 10.24us
<b>Noise (<math>C_{\text{DET}}=50\text{pF}</math>, Gain_integ=2mV/fC, Gain_CDS=32, ADC=9bit)</b>	$\leq 1200 e^-_{\text{RMS}}$ referred to input	Measured Noise depends on systems noise performance
<b>Noise (<math>C_{\text{DET}}=50\text{pF}</math>, Gain_integ=2mV/fC, Gain_CDS=8, ADC=14bit)</b>	$\leq 1400 e^-_{\text{RMS}}$ referred to input	Measured Noise depends on systems noise performance
<b>Noise (<math>C_{\text{DET}}=50\text{pF}</math>, Gain_integ=2mV/fC, Gain_CDS=1, ADC=14bit)</b>	$\leq 2300 e^-_{\text{RMS}}$ referred to input	Measured Noise depends on systems noise performance

Table 4: ISC9717 Specification and Performance (2 of 2)

The ROIC has a multistage pipelined architecture to achieve state-of-the-art performance. Each of the 128 channels in the device contain four major stages:

- A low noise charge integrator with programmable gain
- A low pass filter (LPF) with programmable time constant
- A correlated double sampling amplifier (CDS) with programmable gain
- A programmable ADC (9 to 14 bits gray-codes output)

These stages are shown graphically in Figure 1. Each stage of the channel supports selectable parameters to optimize it for a given application.

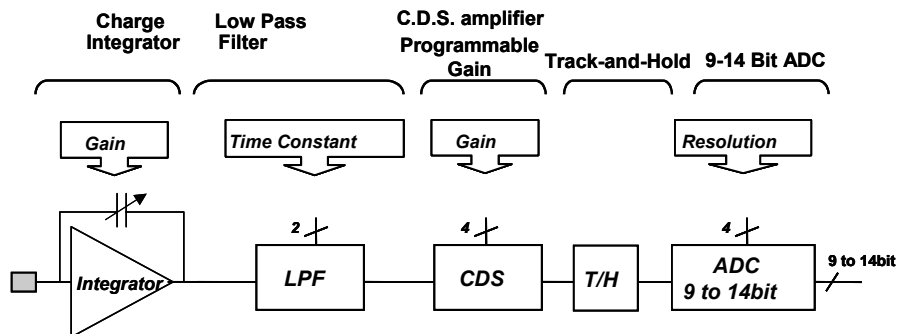


Figure 1: Block diagram of the ISC9717

The charge integrator input stage integrates charge on its feedback capacitor. Its gain is programmable with 2-bit control, as shown in Table 5. The integrator DC offset needs to be adjusted for electron (default) or hole collection.  $V_{OFF\_INTEG} = 1.5V$  for electron collection and  $V_{OFF\_INTEG} = 3.5V$  for hole collection. The overall internal gain is given by  $GAIN = Q_{IN} / C_F \times CDS\_GAIN$ . The ADC input dynamic range is 3V.

GAIN[1-0]	$C_F$	INTEGRATOR GAIN
0 0	0.5pF	2mV/fC
0 1	1pF	1mV/fC
1 0	2pF	0.5mV/fC
1 1	4pF	0.25mV/fC

Table 5: Integrator programmable gain

The low pass filter (LPF) limits the ISC9717 bandwidth to reduce and optimize the thermal noise contribution of the integrator, controlled by 2 bits, LPF\_BIT[1-0], as shown in Table 6.

LPF_BIT[1-0]	LPF Time Constant
0 0	0.8us
0 1	1.3us
1 0	2.8us
1 1	3.3us

Table 6: Low Pass Filter programmable time constant

The correlated double sampling amplifier (CDS) removes the offsets and kTC noise of the integrator stage and reduces the ROIC 1/f noise. The CDS has a programmable gain as shown in Table 7.

CDS_BIT[3-0]	CDS Gain
0000	x1
0001	x2
0011	x4
0111	x8
1111	x32

Table 7: Correlated Double Sampling gain control

The A/D converter for each channel is a single-slope converter. The A/D resolution is programmed with the serial command register bits RAMP[4-0]. The slope is adjusted for a given resolution by using the  $V_{ADJ\_RAMP}$  input pad to the voltage levels shown in Table 8. The ADC output format is Gray-Code. The Gray-Code output for a channel exceeding the ADC range (out-of-range output) is 0, i.e. (0000...0000).

RAMP[4-0]	ADC Resolution	$V_{ADJ\_RAMP}$
00000	9 bit	0.8V
00001	10 bit	0.8V
00011	11 bit	0.6V
00111	12 bit	0.5V
01111	13 bit	0.5V
11111	14 bit	0.45V

Table 8: ADC resolution control bit

The data output signal of the ISC9717 is formatted as 14 bits of Gray-Code, single ended, parallel, current-mode outputs. Current mode outputs allow the user to limit the output voltage swing and reduce the induced switching noise. A PMOS open-drain transistor generates the current output signals; 0mA or 0.6mA for state 0 and 1 respectively. Figure 2 shows a suggested circuit to readout the current output signal; a pull-down resistor ( $R_{load}C_{load} < 5ns$ ) followed by a fast comparator..

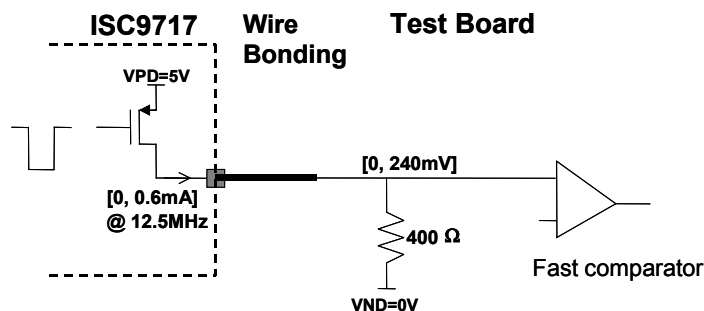


Figure 2: Suggested Output Readout Circuitry

### 3. OPERATION AND SELECTABLE MODES

The ISC9717 has two operational modes, the Default Mode and the Command Mode. The Default Mode allows users to operate the device in a straightforward manner without programming the serial control register. Parameters of the chip are set to fixed values at power up and support electron collection, full 128-channel readout, fixed gains, and 9-bit ADC resolution.

Command Mode allows the user to set parameters specific to their application by sending digital serial commands to the ROIC. In Command Mode the user can set the chip to collect electrons or holes, perform pixel averaging where two adjacent channels are averaged together and read out, set gains of the integrator and correlated double sampling stage, set low pass filter constants, perform a calibration on any or all channels of the device, select the ADC resolution from 9 to 14-bits, and choose an integrate-then-read or integrate-while-read mode depending on requirements for noise and frame rate. Input control signals for Command Mode operation are a Master Clock (CLK), a Synchronization signal (SYNC) and a serial Data Input (DATA\_IN). Table 9 lists the DATA bit definitions and range of values that can be set by the bits of the serial command register. Default values represent the configuration of the ROIC in Default Mode.

BIT(s)	Function	Definition	Default
IWR/ITR	Integration mode	IWT/ITR = 1: Integrate Then Read mode	0 (IWR)
MAMM	Hole collection (Mammography)	MAMM=1 : Hole collection mode enabled	0 (Electron collection)
PIXAVG	Pixel averaging	PIXAVG = 1 : Two columns are averaged	0 (no averaging)
RDIR	Readout direction	RDIR = 1 : Readout is Right to Left (127 to 0)	0 (Readout is Left to Right)
CAL_EN	Calibration mode	CAL_EN = 1 : Calibration mode enabled	0 (Calibration mode disable)
GAIN(2-0)	Integrator gain select	See Gain code definition	000 ( $C_f = 0.5pF$ )
LPF_BIT(1-0)	Low Pass Filter time constant	See LPF code definition	00 ( $T_{LPF} = 1\mu s$ )
CDS_BIT(3-0)	Correlated Double Sampling gain	See CDS code definition	0000 (CDS gain =1)
RAMP(14-10)	Ramp Bit Resolution	See Ramp Gain code definition	00000 (Ramp for 9bit ADC)
CAL (0-6)	Calibration address	[000000] = channel0, [111111]=channel127	0000000 (address 0)
CAL_ODD(6)	Cal Register Odd addresses	CAL_ODD = 1 : odd channel activated	0 (disable)
CAL_EVN(5)	Cal Register Even addresses	CAL_EVN = 1 : even channel activated	0 (disable)
PIX_TST	Pixel Average test mode	PIX_TST = 1 : All columns read out	0 (disable)
VADD(3-0)	VET address	See VET address definition	0000 (VET output grounded)

Table 9: Command Register DATA Bit Definitions

### 3.1. Integrate-While-Read Mode

When the DATA bits of the Serial Control Register are set to Integrate-While Read Mode (IWR), the readout, analog-to-digital conversion, and detector charge integration are performed simultaneously. In this mode, three SYNC cycles are required to integrate, convert and read out the signal from one set of 128 pixels (one line). During the first SYNC cycle, Figure 3, the signal from the detector is integrated and held on a Track-and-Hold capacitor. The ADC conversion of the integrated and held signal occurs during the second SYNC cycle while the next line of detector signals are integrated. The digitized signal is read out during the third SYNC cycle. Using a 12.5 MHz CLK rate, the line time is 34.88us with 9-bit ADC resolution, 55.36us for 10-bit ADC resolution and 670us when the ADC is set to 14-bit resolution.

For systems in which the detector is not gated, i.e. the detector continuously transfers charge to the readout circuit, the integration time starts at the falling edge of the integrator's reset signal RST\_INTEG and the falling edge of the Track-and-Hold signal, T/H. The ADC conversion time is defined as:  $2^N / (2 \times f_{CLK})$  where N is the ADC resolution and  $f_{CLK}$  the master clock frequency (typically 12.5MHz). The integration time will be a function of the programmed ADC resolution. For a given ADC conversion resolution, the integration time can be controlled (increased) by reducing the master clock frequency. If longer integration time is desired, the master clock can be stopped for a period of time during the integration time, before the ADC conversion starts.

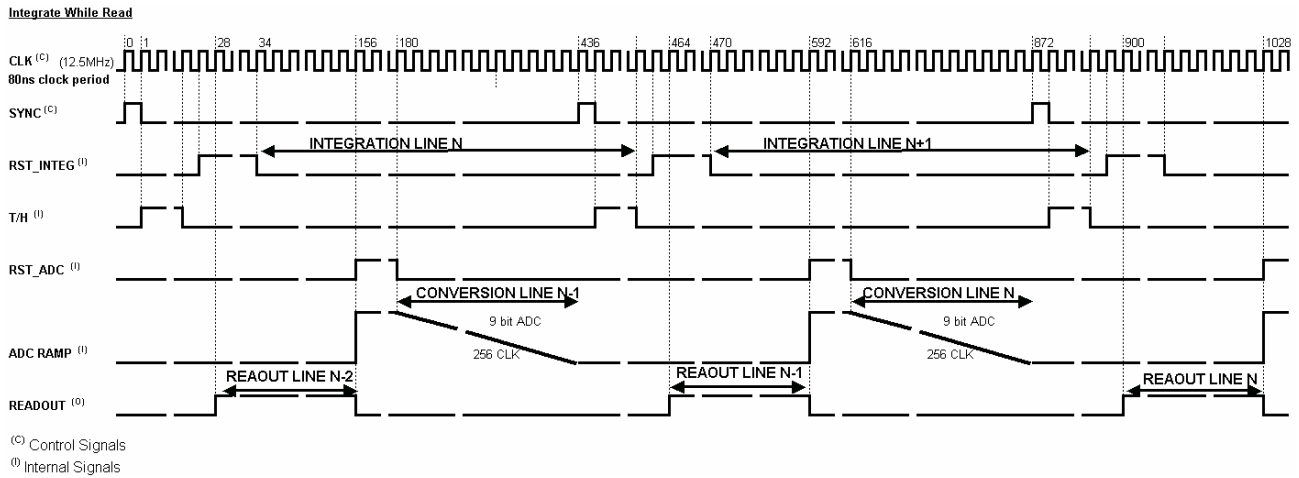


Figure 3: Integrate-While-Read Timing Diagram

### 3.2. Integrate-Then-Read Mode

Setting the ISC9717 to the Integrate-Then-Read mode causes the detector charge integration, analog-to-digital conversion, and readout operations to be performed sequentially, without overlap in time. This mode minimizes coupling for optimum noise performances and increases the line time by the ADC time plus the readout time, which is nominally 31usec. For operation with a 12.5MHz CLK, the line time is 66.08us for 9-bit ADC resolution and 701us for 14-bit ADC resolution. Detector signal from one set of 128 pixels (1 line) is integrated then converted in one SYNC cycle and read out in the next SYNC cycle.

Figure 4 shows the timing of the ITR mode. The first SYNC pulse shown in the diagram starts readout of LINE 0, followed by the integration for LINE 1, and finally the A/D Conversion for LINE 1. The second SYNC pulse shown in the diagram starts the readout of LINE 1, followed by the integration of LINE 2, and finally the A/D conversion of LINE 2.

In the ITR mode, the integration time can be controlled (increased) by reducing the master clock frequency. If longer integration time is desired, the master clock can be stopped for a period of time during the integration time, before the ADC conversion starts.

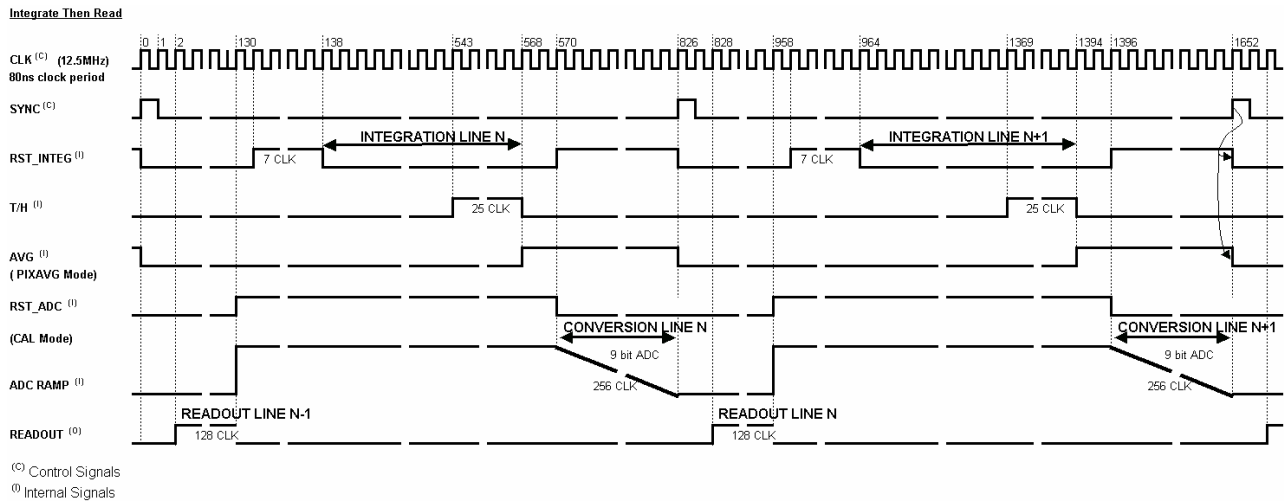


Figure 4: Integrate-Then-Read Mode Timing.

### 3.3. Hole Collection

In the hole collection mode (also called mammography mode due to the hole collection from the Selenium conversion), the ISC9717 is programmed to read holes from Selenium based TFT arrays (CsI TFT arrays generate electrons). The LPF has to be preset during this mode to read the opposite polarity signal. The DC operation points (i.e. external offset voltages) have to be adjusted accordingly for the optimum dynamic range (Table 10).

The response of the circuit to injected charge is opposite that of when electrons are collected.

Thus, the output baseline (no signal in the hole collection mode), to be converted by the ADC, will result in high output counts and is to be considered the offset. The calculation of the normalized output is done by subtracting the signal image from the dark image (or no-signal image). The acquisition and processing of an image should be:

- 1-Acquire the “dark” image
- 2-Acquire the signal image
- 3-Output = Signal image - Dark Image

MODE	MAMM bit	V <sub>OFF INTEG</sub>	V <sub>OFF CDS</sub>
Electron Collection (Default)	0	1.5V	3.5V
Hole Collection	1	3.5V	1.5V

Table 10: Electron and Hole collection adjustment

### 3.4. Pixel Averaging Mode

The ISC9717 is externally programmable to average the signal of two adjacent channels when the detector is in the 2lp/mm spatial resolution (2 pixels binned together), Figure 5. Every other channel is read out. In the average mode (PIXAVG=1), 2 pixels are binned together to improve the signal/noise ratio and increase the readout speed of the array. The resulting average output is  $(V_1+V_2)/2$ .

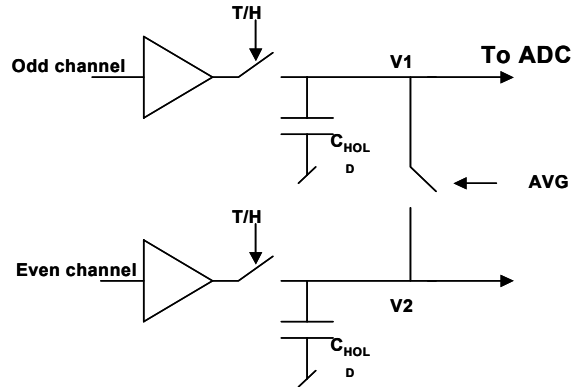


Figure 5: Averaging function

### 3.5. Readout Direction

The ISC9717 is designed to support applications such as flat panel arrays and scanning systems where multiple ROICs are abutted vertically along one or two sides of the detector array as shown in the example of Figure 6. In this example, the detector array is split into two parts, using ISC9717 chips on each side. Half of the columns will readout by each of the half array. Also shown in Figure 6 is the connection from the TFT array to the input of the ROIC. In order to acquire the image of the entire array without any image order inversion, the readout direction must be externally programmed using the serial command register. ROICs on the left side would be programmed to readout from left to right and ROIC on the right side of the array would be programmed to readout from right to left. The external pin REVERSE sets the readout direction (in the default mode)

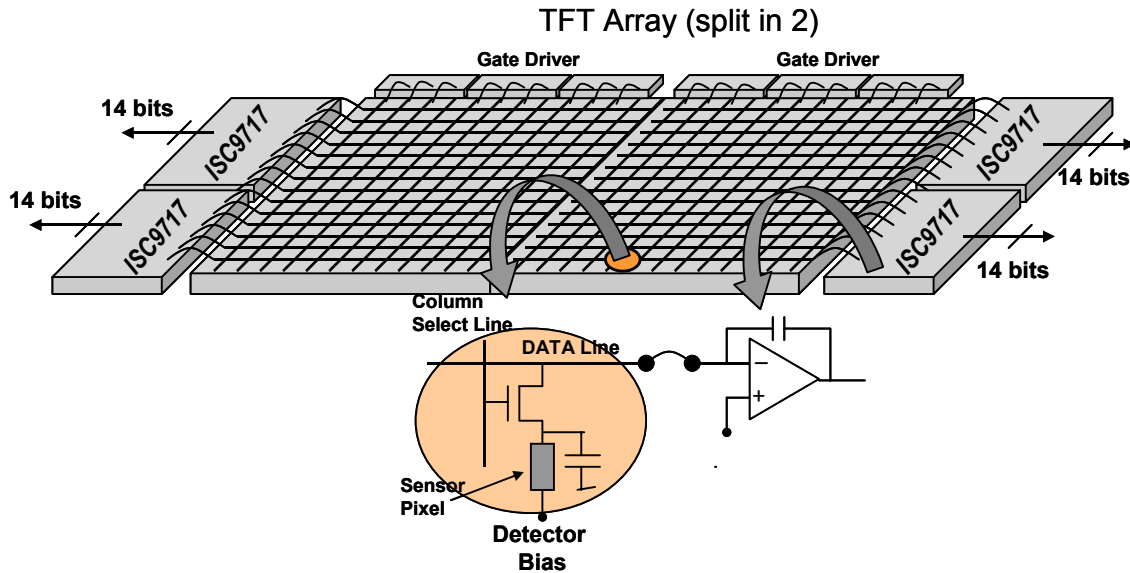


Figure 6: Example of Flat Panel Array Configuration and TFT Interface to the ROIC Input

### 3.6. Internal Test Calibration Mode

The chip has an on-chip charge injection circuit, primarily used as a test input, shown in Figure 7. The calibration mode allows the injection of a programmable charge to any given channel, to every odd channel or every even channel, or to all channels (7 bit address + 2 bits odd/even). The injected charge is adjusted by an external DC voltage, set by the input pad  $V_{CAL}$ . The internal charge injection can be used for gain and linearity tests of the device. The amount of charge injected is given by:  $Q_{CAL} = C_{CAL} (V_{POS} - V_{CAL})$ , with  $C_{CAL} = 0.5\text{pF}$ .

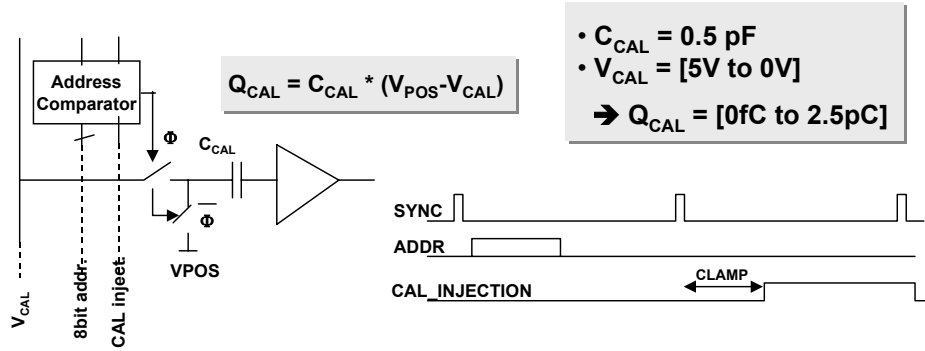


Figure 7: On-chip Test Calibration Circuit

#### 4. PHYSICAL DESIGN AND SYSTEM INTERFACE

A commercial silicon foundry is used to fabricate the devices in a standard 0.5µm process with double metal and double poly-silicon layers. The die size is 11.15 x 4.74mm<sup>2</sup> to edge of scribe lane. The wafer size is 200mm (8-inches) resulting in 487 die per wafer. Figure 8 shows the pad locations of the ISC9717. All the input pads are on the top edge and all the bias, clock, and output pads are located on the bottom edge of the die. The staggered input pad allows wire bonding or other type of interface connections such as Tape Automated Bonding (TAB). The input pad pitch is 80µm (from passivation opening). The passivation openings are 80x150µm<sup>2</sup>. The 80-micron pitch was selected to interface with TFT arrays having a pitch of 130 microns or less.

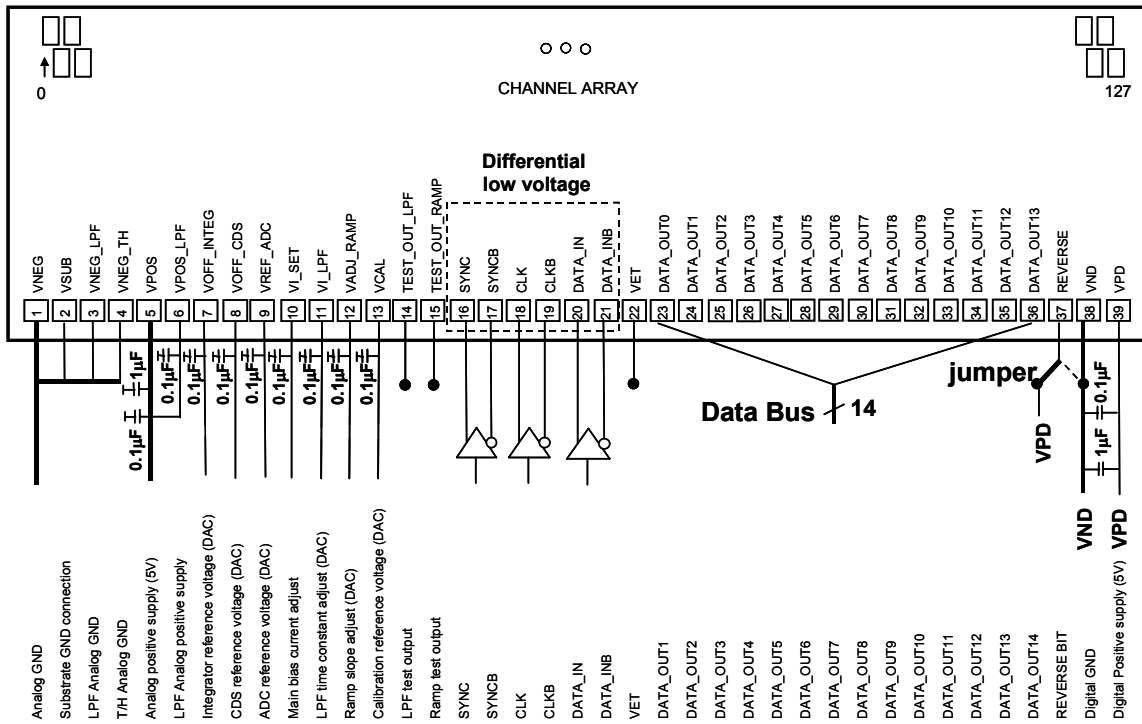


Figure 8: ISC9717 pad locations and interface

## 5. TEST RESULTS

### 5.1. ISC9717 Settings

Characterization testing was performed on twenty ISC9717 chips. These devices were wire bonded in 84-pin LCC packages for testing. The data used in the characterization was confirmed from ten parts. Gray code outputs were converted into binary counts. When output voltages were displayed, the output voltage was calculated as:  $V_{out} = [\text{Output count (binary)}] \times 3V / 2^{\text{BIT\_ADC}}$ . Offset corrections were applied to characterization tests when appropriate. The offset of every channel (no charge injection) was first measured and stored, then subtracted from the final output value.

The ramp control voltages (VADJ\_RAMP) were adjusted as shown in Table 8 within the different ADC conversion ranges selected. These values were set to adjust the ramp dynamic range to 3V over the ADC conversion time.

### 5.2. Output data timing

Figure 9 shows the readout timing in the ITR mode. The acquisition of the output bit should occur during the falling edge of the master clock due to expected delay. However, with test hardware delays, the system was timed to acquire about 20ns after the rising edge of clock. Output data were readout at the nominal rate of 12.5MHz.

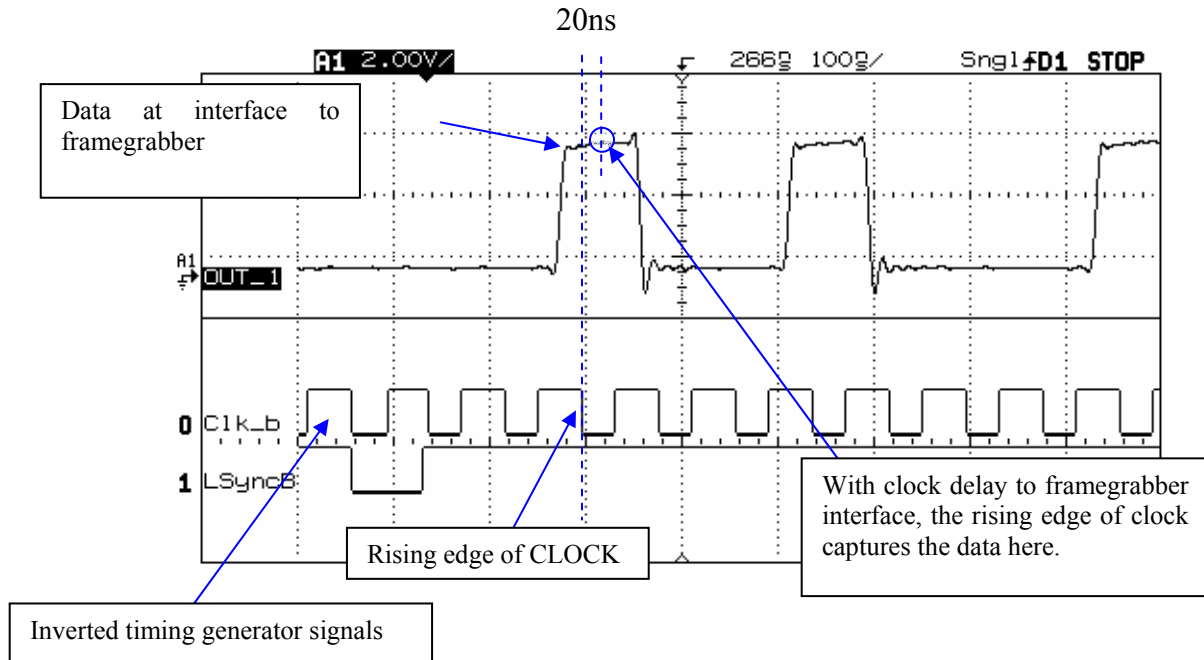


Figure 9: Output data timing

### 5.3. Characterization Test Summary

The ISC9717 ROIC designed for medical and industrial X-ray detector systems has been fully characterized. A summary of the ISC9717 performance against the specification requirements is given in Table 12.

Parameter	Specification/Design	Measurement	Test Compliance
Temperature of Operation	10 to 40 °C	Characterized at room temperature (30 °C)	✓
Clock Frequency	12.5MHz (80ns period)	All tests at 12.5 MHz (master clock)	✓
Input Signal (CLK, SYNC, DATA)	$\geq \pm 50\text{mV}$ differential	$\pm 50\text{mV} \leq \text{signal} \leq \pm 400\text{mV}$ (+400mV=pseudo-ECL)	✓
	1V < signal < 4V	1V < signal < 3.5V (for signals $\geq \pm 100\text{mV}$ )	
	Rise/fall time $\leq 10\text{ns}$	Rise/fall time $\leq 10\text{ns}$	
Internal Signals (VET)	Functionality Test	Functional	✓
Power consumption	< 256 mW / chip < 2 mW / channel	< 204 mW / chip < 1.6 mW / channel	✓
Dark Image Acquisition	None	58mV < Offset < 96mV	n/a
Flat Field Acquisition	None	Uniformity < 38mV	n/a
Readout Rate	12.5 MHz	12.5 MHz	✓
Data Line Driving Capability	Cline < 10 pF	Tested with Cline $\leq 15\text{pF}$	✓
Output Signal	0.4mA to 0.6mA (absolute value +/- 20%)	Absolute value ~0.61mA	✓
	Dispersion $\leq \pm 10\%$	Dispersion $\leq \pm 10\%$ (channel to channel and chip to chip)	✓
Integrator Gain linearity	2, 1, 0.5, 0.25 V/pC Gain linearity $\leq 1\%$	1.79, 0.9, 0.46, 0.22 V/pC Gain linearity < 0.4%	✓
Correlated Double Sampling Gain linearity	Programmable gain x1, x2, x4, x8, x32 Gain linearity < 1%	Gain linearity < 1%	✓
Gain Dispersion	None	Channel-to-Channel < 0.7% Chip-to-chip < 1.1%	n/a
Readout Direction	Reverse readout direction	Functional	✓
ADC Resolution	9 to 14 bits True 12bit (goal 14bits) Gray code output	Characterization limited by injection circuit	Cannot be measured directly
ADC Linearity	+/- 0.5 LSB	Characterization limited by injection circuit	Cannot be measured directly
ADC Step Rate	25MHz (12.5MHz master clock rate) True 12bit (goal 14bits)	Characterization limited by injection circuit	Cannot be measured directly
ADC Ramp Adjustability	Functionality Test	Functional	✓
LPF Time Constant	1us, 2us, 4us, 5us (Design Goal)	0.8, 1.3, 2.8, 3.3 us	Not Guaranteed
Crosstalk (internal to ROIC)	$\leq + / - 0.25\%$	< 0.1 %	✓
Pixel Averaging	Averaging 2 adjacent channels	Functional	✓
Mammography Mode	Hole collection from detector	Functional	✓
Dynamic Range	None	$\geq 2.87\text{ V}$	n/a
Noise (9bit, CF=0.5pF, CDS=x32, Cdet=50pF)	ENC $\leq 1000\text{ e-RMS}$ (Goal)	ENC < 1200 e-RMS	Measured but not Guaranteed
Noise (14bit, CF=0.5pF, CDS=x1, Cdet=50pF)	ENC $\leq 2000\text{ e-RMS}$ (Goal)	ENC < 2300 e-RMS	Measured but not Guaranteed

Table 12. Specifications and Measurements

## 6. CONCLUSION

The ISC9717 is an off-the-shelf readout integrated circuit for digital X-ray imaging applications and instrumentation using solid-state detectors. The ISC9717 is a high performance, low-noise, 128-channel, fully programmable ROIC with a 9 to 14-bit programmable A/D converter per channel. The 80-micron input pitch allows the interface of the ROIC via wire bonding, TAB or flip-chip hybridization techniques to a TFT arrays or segmented solid-state detectors (Si, CdZnTe, GaAs or Ge).

The ROIC is fully programmable via its serial control interface. The integrator and correlated double sampling stages gain control allow the optimization of the dynamic range from 300,000 carriers (48fC) to  $75 \times 10^6$  carrier (12pC). The averaging function implemented allow the binning of 2 adjacent pixels improving the signal to noise ratio and reducing the readout time for higher frame rate applications. Each channel has its own programmable A/D converter from 9 to 14 bit resolution allowing the trade off between signal resolution and frame rate for dynamic X-ray imaging systems.

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