

Very Wide Dynamic Range SWIR Sensors for Very Low Background Applications

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ABSTRACT

This paper describes a high performance 320 by 256 readout integrated circuit (ROIC) designed for P-on-N short wave infrared (SWIR) detectors including InGaAs and HgCdTe, which also has the ability to operate at low input current levels with N-on-P detectors. The ROIC/FPA will support a wide range of system requirements from very low background applications (nightglow) to daytime high illumination conditions. To accommodate the wide scene dynamic range requirements, two selectable integration capacitors are used to control the input circuit transimpedance gain. A 10fF integration capacitor is used for low noise and low flux levels down to 10^{-5} ft Lambert, corresponding to approximately 2×10^{10} ph/cm²-sec for 0.9 μ m to 1.7 μ m spectral band using f/1.5 optics, assuming a 2856 Kelvin blackbody distribution. For higher flux levels, a 0.21pF integration capacitor can be selected, thus providing over a factor of 20 dynamic range. A capacitive feedback transimpedance amplifier (CTIA) provides a low noise detector interface circuit capable of operating at low input currents without frame-to-frame image lag. A sample and hold capacitor is also part of the input unit cell architecture, which allows the FPA to be operated in full frame snapshot mode and provides the maximum integration time available. The integration time is electronically controlled (gated) by an external clock pulse, and is adjustable from 0.5 μ sec to approximately the frame time of 33.3msec for 30Hz operation. This produces an additional factor of 66,000 to the total system dynamic range. The combination of integration time control and selectable integration capacitors accommodates over nine orders of magnitude in scene dynamic range.

Keywords: SWIR Sensor, ROIC, Readout Integrated Circuit, P-on-N Detectors, N-on-P Detectors, SWIR HgCdTe Detectors, InGaAs Detectors, Gated Integration, Capacitive Feedback Transimpedance Amplifier, CTIA

1. INTRODUCTION

The performance of nighttime low light level imaging systems can be greatly enhanced by extending their spectral sensitivity into the short wave infrared (SWIR) or near IR region. Atmospheric nightglow from 1.3 μ m to 1.8 μ m can provide adequate illumination for near IR imaging systems that operate at room temperature or temperatures compatible with a single stage thermoelectric cooler. However, in the daytime, the intensity of solar scattered illumination can be seven to eight orders of magnitude higher and thus a readout integrated circuit (ROIC) designed for high performance near IR systems must also be able to handle this wide input signal range. In addition, there has recently been a great deal of interest for active near IR imaging systems that use pulsed laser illumination and gated integration. For these applications, the key ROIC design challenges are to integrate the required detector interface circuitry into the desired pixel pitch area and provide low noise, high transimpedance gain, high bandwidth, and dynamic range with low power dissipation. This paper describes a 320 by 256 ROIC (ISC9809) incorporating these features for near IR imaging systems using P-on-N InGaAs or HgCdTe detector arrays. The ISC9809 is designed to be physically and electrically compatible with the Indigo Systems Corporation ISC9705 Standard 320 ROIC¹ and thus has many of the same programmable operating modes such as dynamic image transposition, dynamic windowing, selectable number of outputs, variable signal gain, input charge skimming, and on-chip power adjustment.

The ISC9809 has a number of additional features that make it ideal for high performance SWIR or near IR applications. Although it was designed for P-on-N detectors it can also be used with N-on-P detector arrays (HgCdTe or PtSi) operating at low input current levels. It incorporates six integration/readout modes that are used to support a wide variety of applications. In particular, it has a gated snap shot integration mode for systems using pulsed laser illumination. The integration period can be synchronized to a laser pulse and the integration time can be set to 0.5 μ sec or longer. For astronomy applications that require very low noise and have long integration times at under low background conditions, this ROIC has an operating mode

that is ideal for Fowler Sampling² of the integrated signal. A simple digital command word allows multiple readouts of the integrating signal during the integration period. This nondestructive multiple correlated sampling technique is used to improve the noise performance for these very low background applications.

2. UNIT CELL DESIGN

Near IR system requirements present many challenges to the readout integrated circuit design. The input circuit not only provides the detector interface to the readout multiplexer but it often sets the performance limits for the entire focal plane array. An objective of this project is to design a ROIC capable of supporting a variety of SWIR or near IR imaging applications. The capacitive feedback transimpedance amplifier (CTIA) input offers the best overall performance characteristics including read noise, signal bandwidth, and power dissipation to meet this goal. In addition, a CTIA input circuit does not have image lag (frame to frame image smearing) even at very low input current levels. This problem is sometimes observed with other types of low light level input circuits. Also, the CTIA provides a stable detector bias voltage that is independent of detector current, produces a very linear signal response to input current, and has adequate signal bandwidth to support pulsed laser applications that require a gated integration.

The unit cell design used in this ROIC is shown in Figure 1. It is fabricated using 0.6 μ m CMOS process incorporating double poly and triple metal in a 30 μ m by 30 μ m pitch. To accommodate the wide scene dynamic range requirements, two selectable integration capacitors are used to control the input circuit transimpedance gain. A 10fF integration capacitor is used for low noise, low background levels below 1×10^{10} photons/cm²-sec. For higher flux levels, a 210fF integration capacitor can be selected by using the programmable Control Register feature of this ROIC or by applying a logic level to the GAIN pad. The CTIA amplifier bandwidth is also selectable using two bits in the programmable Control Register or by applying a logic signal to the BWL pad.

Each unit cell contains a sample and hold capacitor to allow the FPA to operate in a full frame snapshot integration mode. The integration time is electronically controlled by an external clock pulse length and is adjustable from approximately the frame period to as short as 0.5 μ sec for gated integration applications. The combination of selectable integration capacitance and integration time will accommodate over nine orders of scene dynamic range.

The CTIA amplifier bias current can be adjusted using six bits in the Control Register. The default or nominal amplifier bias current is 100nA, but it can be adjusted from 3nA to 350nA using the programmable features of this ROIC. This input amplifier also has a charge skimming feature that allows a variable amount of charge to be skimmed “off” or skimmed “on” during the integration period. The skimming feature allows this input circuit to be used with either P-on-N or N-on-P detectors.

The CTIA amplifier input circuit also has an anti-blooming gate that prevents the input circuit from saturating and prevents the detector from debiasing even under very high saturating background conditions.

The predominant noise sources in this ROIC are associated with the unit cell circuit. These are the CTIA amplifier noise and kTC noise associated with resetting the integration capacitor. The CTIA amplifier noise is driven by the detector capacitance and the predicted noise performance of this input circuit is approximately 48 electrons when operating at 250 Kelvin with detectors having a capacitance of 0.1pF or less.

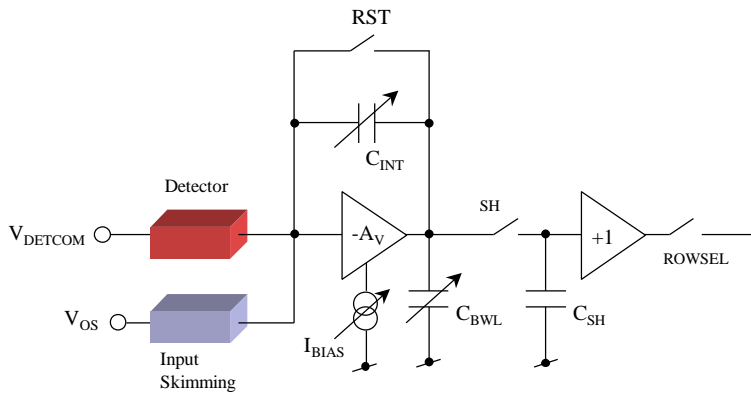


Figure 1. Simplified schematic of unit cell input circuit.

3. COMMAND MODE OPERATION

The ISC9809 readout contains a programmable Control Register that is very similar to the Control Register in the Indigo Systems Corporation ISC9705 Standard 320 ROIC. This Control Register is used to select the operational modes and features of the ROIC. Figure 2 illustrates the serial Control Register and the readout functions it supports. To operate in this Command Mode, a serial 32-bit DATA word is input through the DATA pad. This allows access to all the advanced features such as windowing, image transposition (invert/revert), selectable number of outputs, on-chip power bias control, gain select, CTIA amplifier bandwidth selection, input skimming, and the special integration/readout modes. Master clock frequencies up to 5 MHz (10 MHz output pixel rate) are supported when operating at room temperature in the Command Mode. The total number of required interconnects is 12-19 depending on the number of outputs and other options invoked. Data bits loaded into the control register determine the operating modes for the readout during the next frame's integration and readout. A new control word is only required when the settings or readout functions need to be changed.

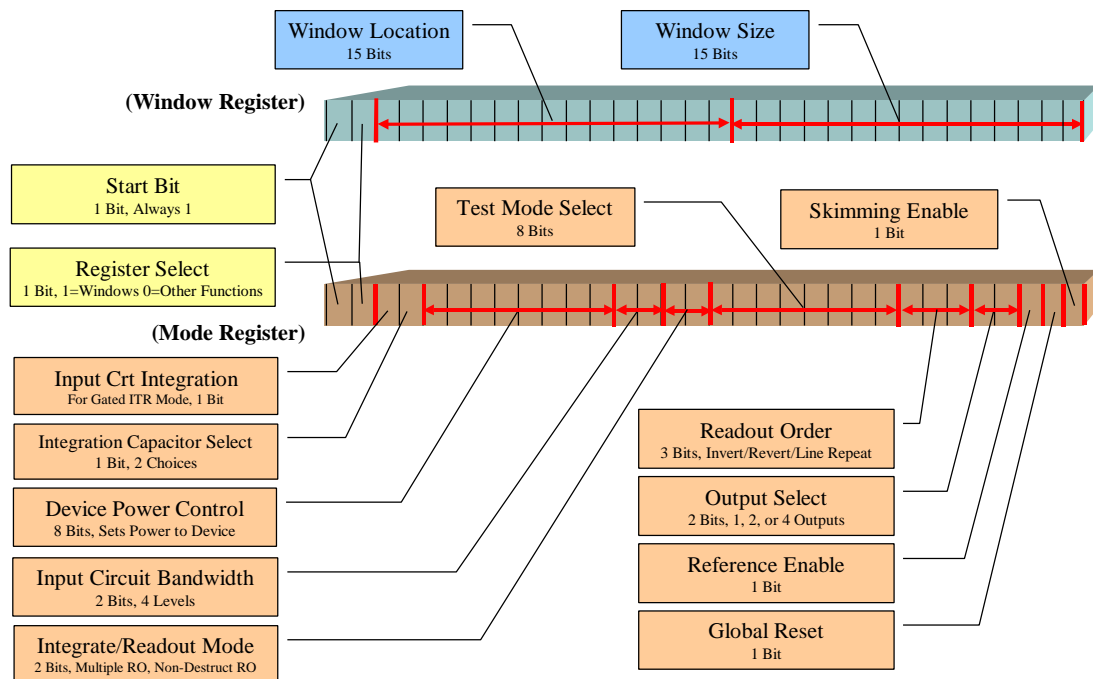


Figure 2. ISC9809 Serial Control Register.

Figure 3 shows a block diagram for Command Mode operation. Each unit cell CTIA input circuit contains an anti-blooming transistor. A sample and hold capacitor in the unit cell holds the integrated signal which is addressed by a column bus line, buffered by a column amplifier, and sampled onto a column sample and hold capacitor. The skimming function provides a global charge to each integration capacitor.

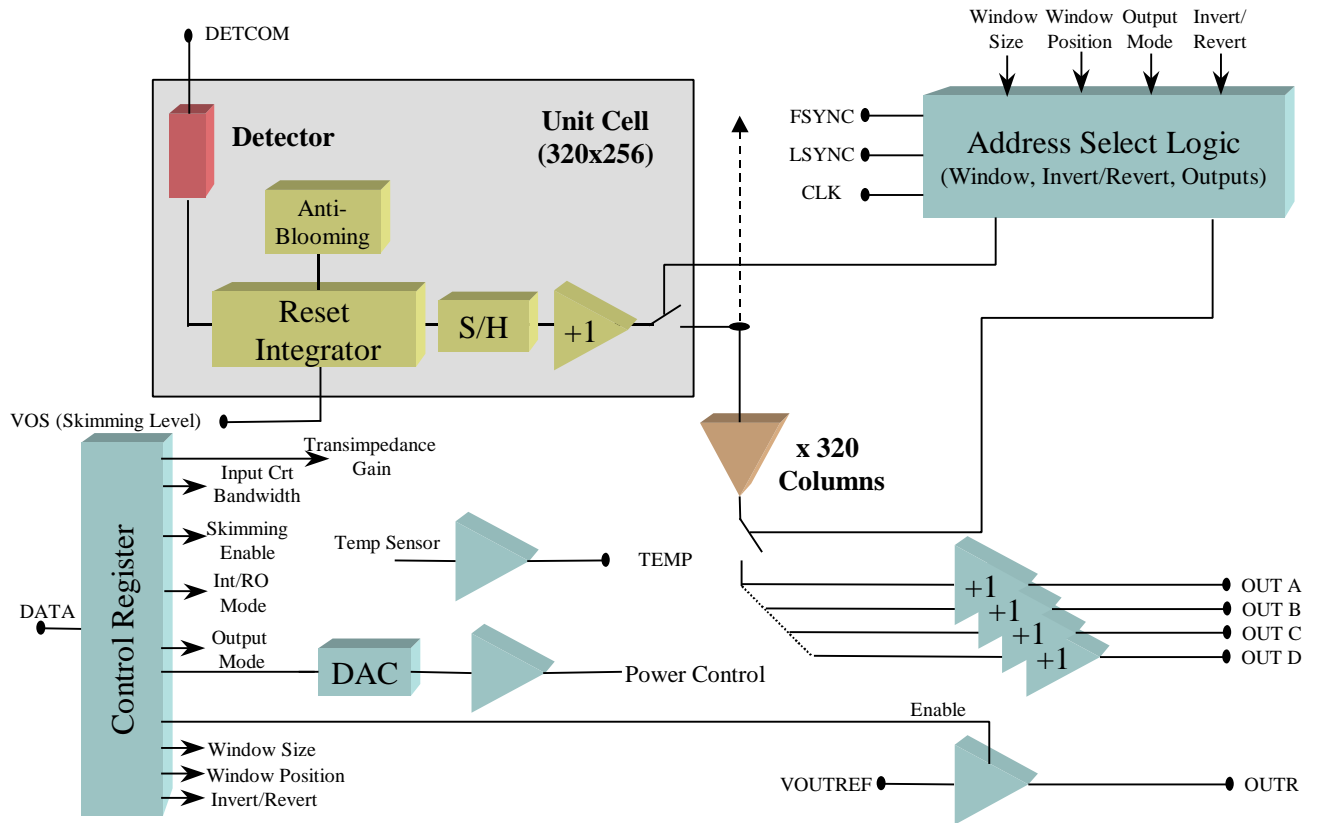


Figure 3. Block diagram for Command Mode Operation.

4. DEFAULT MODE OPERATION

The Default Mode does not use the on chip serial Control Register. When the ROIC is powered up, the device defaults to operation as a standard 320x256 format imager. In Default Mode, the ISC9809 operates with a single output, selectable integration capacitance, selectable CTIA amplifier bandwidth, full window, normal scan order, no reference output, with skimming disabled. This mode is designed to support NTSC or PAL timing, and it provides a simple interface with reduced external electronics for applications that do not require the advanced ROIC features or high frame rate performance. The Default Mode only supports P-on-N detector operation and the standard integration/readout operation. The total required interconnects for this mode of operation is 16. A block diagram for the default mode operation is shown in Figure 4. On-chip power control is accomplished by applying an analog voltage to the IMSTR_ADJ PAD. An on-chip temperature sensor output is also provided in the Default Mode.

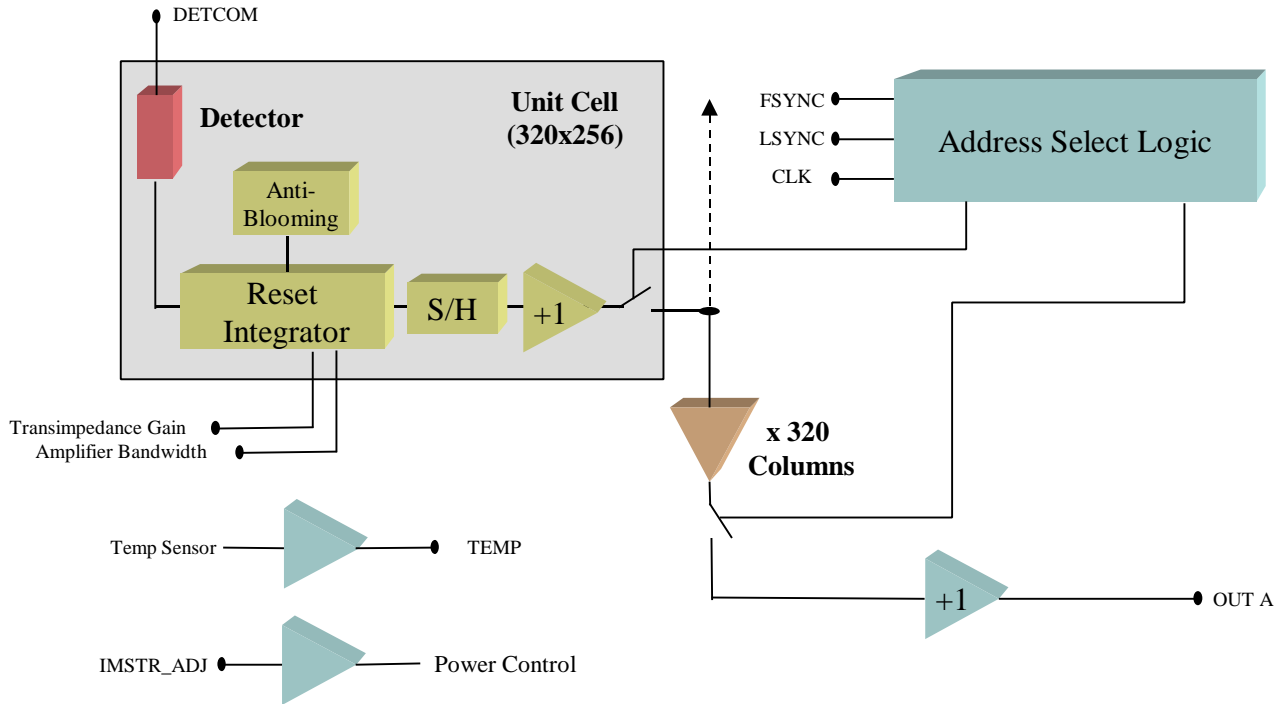


Figure 4. Block diagram for Default Mode Operation.

5. SPECIAL ROIC FEATURES

The output channel selected for a given pixel is determined by the output mode selected. The ISC9809 supports one, two, or four outputs with or without a reference output. In order to invoke an output mode, other than single output with no reference output, the Command Register must be used. For single output mode, all pixels are read out through OUTA. When using multiple outputs, pixels are assigned to one output and will be read out only through that output, regardless of the image transposition (Invert, Revert) and the Windowing Modes selected. Figure 5 illustrates the readout order for the single output mode and the various options for image transposition. The control bits RO1 and RO2 in the Control Register determine this image transposition.

The lowest left-hand pixel is defined as pixel [0,0] when in default mode. This pixel is the first pixel to be read out in the single output mode using all default settings for Invert, Revert, Windowing, and Line Repeat modes. This mode of operation would be chosen for a “normal” inverting optical system. By placing the bottom row [row 0] at the “bottom” of a camera system, and using this type of lens a normal raster scan image will be presented.

When the invert/revert bits are programmed RO[2-1]= 01, the image is read out beginning at [0,255] and finishing at [319,0]. This mode is shown in the upper left section of Figure 5. When the invert/revert bits are programmed RO[2-1]= 11, the image is read out starting from [319,255] and finishes at [0,0]. This mode is shown in the upper right section Figure 5. When the invert/revert bits are programmed RO[2-1]= 10, the image is read out starting from [319,0] and finishes at [0,255]. This mode is shown in the lower right section of Figure 5.

When two outputs are selected, the first pixel is presented at OUTA, and the second pixel is presented at OUTB. Alternate pixels are presented at the A and B outputs respectively. When four outputs are selected, the first pixel is presented at OUTA, the second pixel is presented at OUTB, the third pixel at OUTC, and the fourth at OUTD. Alternating in four pixel increments, pixels are presented at the A, B, C, and D outputs respectively.

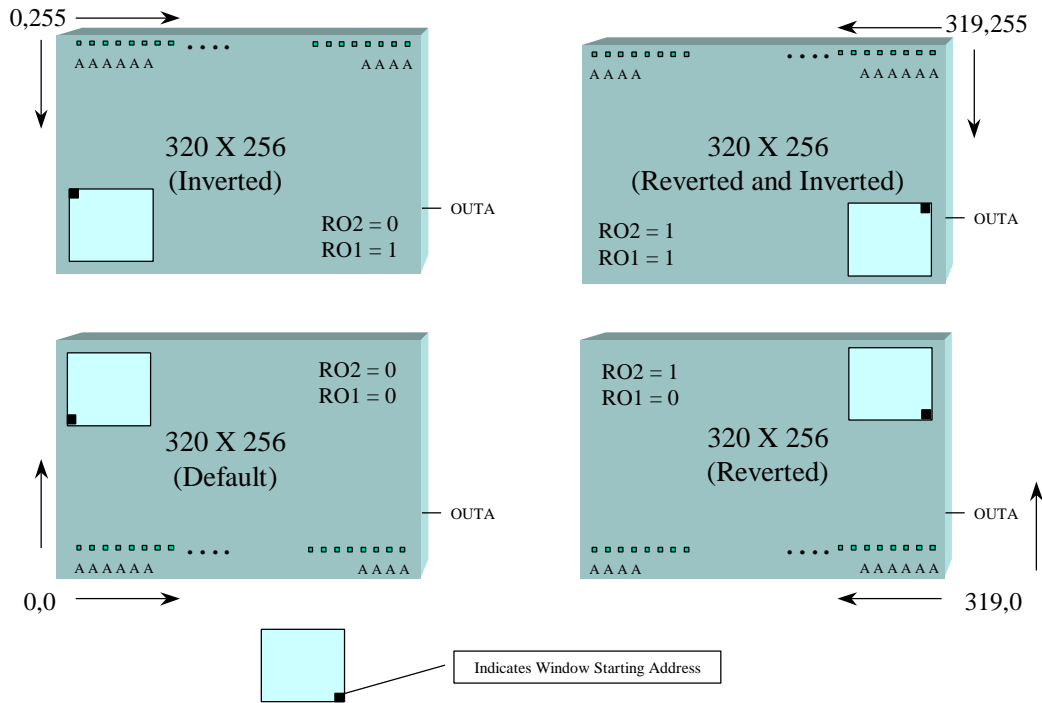


Figure 5. Single output readout order in various Command Modes.

The default window size is the full window 320 by 256. To change the window size, the ROIC must be operated in the Command Mode. The serial Control Register data bits WAX[7-0] and WAY[6-0] define the column and row start addresses respectively. The data bits WSX[7-0] and WSY[6-0] determine the number of columns in the window and the number of rows in the window respectively. The Figure 6 shows a summary of this window mode operation.

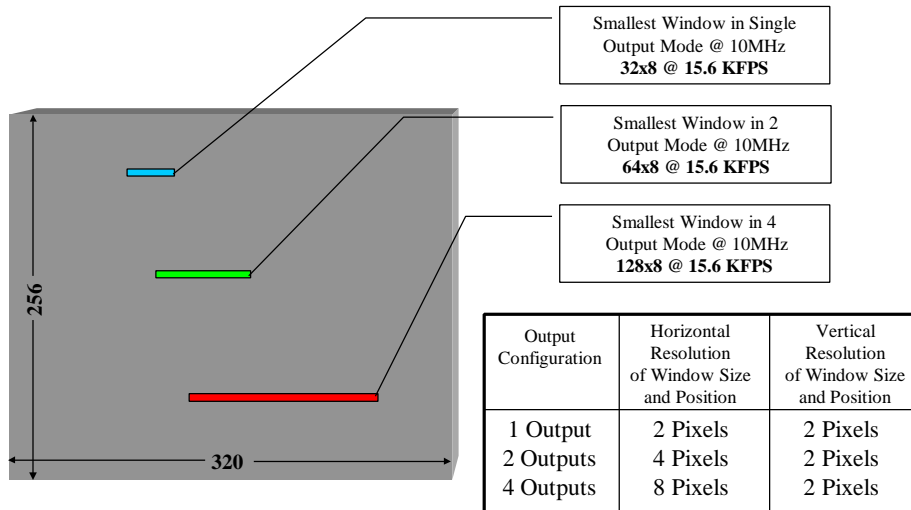


Figure 6. Windowing mode summary.

On-chip bias requirements for the analog signal path circuits are easily adjusted for various applications. These internal bias supplies are shown in Figure 7. The Master Bias Supply is controlled either through three data bits, I[2-0], in the Control Register or by applying an analog voltage to the IMSTR_ADJ pad. This Master Bias can be adjusted +/-50% from the nominal design value. The unit cell CTIA amplifier bias is also controlled by three data bits, AP[2-0], in the Control Register and can be adjusted from 10% to 150% of its nominal design value. The remaining signal path bias controls affect the column bias, column buffer, output multiplexer, and output drivers. Two bits, PWA[1-0], can vary these biases from one-third to twice their nominal design values.

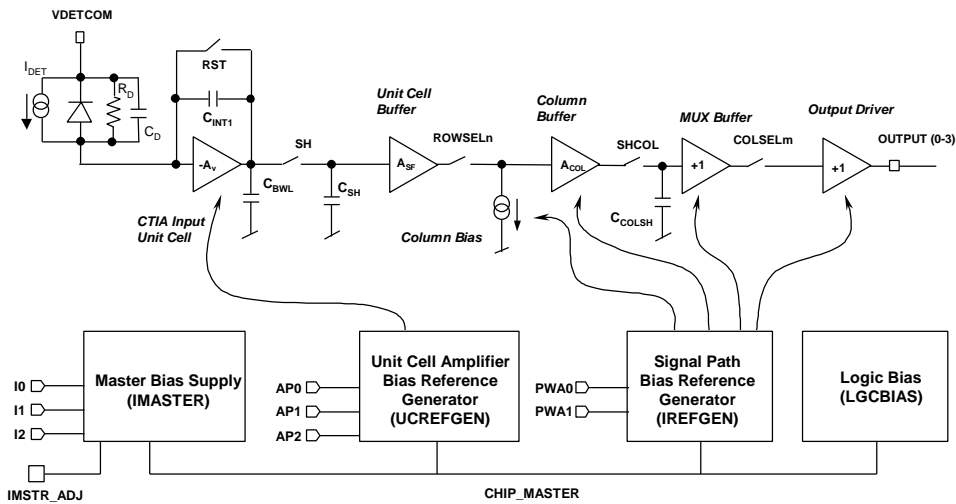


Figure 7. On-chip bias supply controls.

6. INTEGRATION AND READOUT MODES

Six integration/readout modes are available for various applications. Each involves a full frame snapshot integration with all detector signals being simultaneously integrated and simultaneously sample and held. Each of these modes are controlled by the rise and fall of the FSYNC clock pulse. The primary integration modes are Integrate-While-Read (IWR) or Integrate-Then-Read (ITR). The timing patterns for these are shown in Figure 8 and Figure 9 respectively. The rising edge of the FSYNC clock pulse marks the beginning of the frame time. This is followed by a series of LSYNC pulses that produce the readout sequence. LSYNC controls the synchronization of the readout of each individual line. In the IWR mode, the frame time is approximately equal to the readout time. For this mode, the integration time occurs during the readout time, allowing for the greatest possible frame rate and integration time duty cycle (where integration time duty cycle = T_{Int} / T_{Frame}) for a given window size. The minimum frame time can be equal to the readout time.

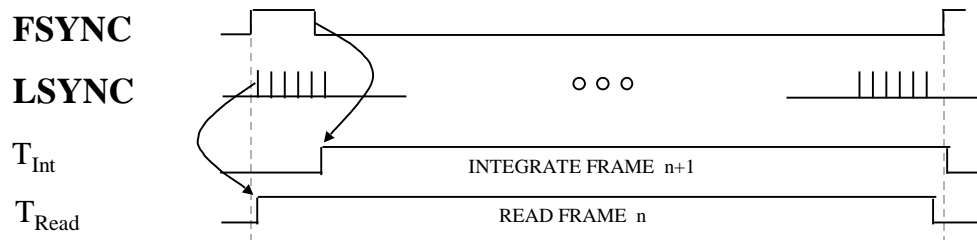


Figure 8. Integrate-While-Read timing.

In the ITR mode, the rising edge of the FSYNC clock pulse marks the beginning of the frame time. This is followed immediately by a sequence of LSYNC pulses that produce a readout sequence. Note that in this case, the FSYNC clock remains high until the readout sequence has been completed. In ITR mode, the integration time occurs after the readout time, producing a frame time that is approximately equal to the readout time plus the integration time. This results in a lower maximum frame rate and integration time duty cycle for a given window size. A potential benefit of this integration mode is for applications that are sensitive to the time delay between integration and readout operation. This mode has the advantage of a fixed time between the end of integration and the start of the readout sequence. Another potential benefit of the ITR mode is that it separates the integration process from the readout process, thus making it nearly impossible for the signals being read out to corrupt the signals being integrated.

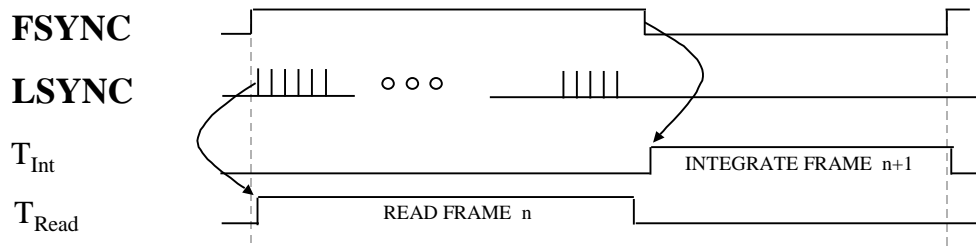


Figure 9. Integrate-Then-Read timing.

The third integration/readout mode is a special version of ITR. It is used to gate the integration process permitting very short integration times from about $5\mu\text{sec}$ to as short as $0.5\mu\text{sec}$ at room temperature or to about $0.25\mu\text{sec}$ when operating the ROIC at cryogenic temperatures. This special gated ITR mode is ideal for pulsed laser applications where the integration and frame readout can easily be synchronized to the laser pulse.

For very low background, very low noise, and very long integration time applications, the integrated signal can be sampled multiple times during the integration period. This integration with multiple readout mode begins with setting the IMRO bit in the command register. The first FSYNC pulse starts the integration and subsequent FSYNC pulses non-destructively sample the continually integrating signal. Each sub-frame image can be read out and the data processed off focal plane to reduce the readout noise.

A fifth integrate/readout mode combines a true snapshot with multiple non-destructive readouts. The final integrate/readout mode reads out every row twice in succession. This mode can be used with any of the above modes and allows the 320 by 256 readout to easily produce RS170 compatible video signals.

7. APPLICATIONS

The ISC9809 ROIC was designed specifically to support room temperature near IR or SWIR applications. With a CTIA input circuit and selectable integration capacitor, this ROIC will support a wide range of system requirements from very low background (nightglow) to daytime illumination conditions. It was designed to interface with HgCdTe or InGaAs P-on-N detector arrays. However, it also is capable of operating with N-on-P detectors (HgCdTe or PtSi) for low background or low detector current applications.

The special gated ITR mode and the CTIA input circuit makes this ROIC ideal for pulsed laser applications. Gated integration times as short as $0.5\mu\text{sec}$ can be synchronized to a pulsed laser for use in active infrared imaging systems.³

Even though this ROIC is designed for room temperature operation, it will have excellent performance for low to mid background SWIR or MWIR applications at cryogenic temperatures. The detector interface for the ISC9809 is identical to

that of the ISC9705 Standard 320, and thus detectors designed for the ISC9705 ROIC (InSb, QWIP, HgCdTe, and InGaAs) will have excellent performance at low to mid backgrounds with the ISC9809.

For astronomy applications or systems operating at very low input signal levels and very long integration times, the nondestructive read capability is important for reducing the readout noise by allowing multiple readouts during the integration time. This multiple correlated sampling of the integrated signal is easily performed using the ISC9809 ROIC.

8. PREDICTED PERFORMANCE SUMMARY

The ISC9809 ROIC is currently being fabricated and a summary of the expected performance is given in Table 1.

Table 1. Expected Performance

Parameter	Performance
Array Configuration	320 (H) by 256(V)
Pixel Pitch	30 μ m x 30 μ m
Well Capacity C _{INT} = 10fF C _{INT} = 210fF	175K carriers 3.5M carriers
Input Current Range Minimum Maximum	< 1fA > 1 μ A
Operating Temperature	Room Temperature to < 80 Kelvin
Total Readout Noise Room Temperature 80Kelvin	~ 50 electrons ~ 25 electrons
Number of Outputs	Selectable 1, 2, or 4
Maximum Output Data Rate	10MHz at Room Temperature
Maximum Frame Rate (Full Frame) One Output Two Outputs Four Outputs	110 FPS 200 FPS 350 FPS
Power Dissipation Minimum (One Output) Nominal (One Output, 10MHz Output Pixel Rate) Maximum (Four Outputs, 10MHz Output Pixel Rate)	< 15mW < 75mW < 150mW
Output Voltage Swing	> 2.5 Volts
Non-Linearity	< 0.1%
Integration Time Minimum Maximum	0.5 μ sec (0.25 μ sec at 80 Kelvin Operating Temperature) ~ Frame Period

9. ACKNOWLEDGEMENTS

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10. REFERENCES

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