

Low Cost 160 x 128 uncooled infrared sensor array

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ABSTRACT

This paper presents a novel low cost, high performance, readout integrated circuit (ROIC) for bolometer uncooled detector applications. The array is designed to offer better than 80mK NE Δ T using f/1.8 optics. The design incorporates advanced on-ROIC signal processing electronics that allows bolometer element non-uniformity control over a wide range of ROIC substrate temperatures. The small format array is ideally suited for high volume low-cost production applications.

Keywords: uncooled, infrared, low cost, bolometer, ROIC, readout integrated circuits

1. INTRODUCTION

A new approach for uncooled infrared readout integrated circuits (ROIC) has been developed. The approach used in this development optimizes cost to performance by using a 160 x 128 readout and achieving 80mK NE Δ T using f/1.8 optics.

Advances in ROIC design greatly reduce system sensitivity to:

- Variations in bolometer mean resistance.
- Bolometer resistance peak to peak variance.
- Variations in bolometer thermal conductance
- Variations in bolometer peak to peak TCR.
- FPA temperature stability.
- Power supply drift and noise.

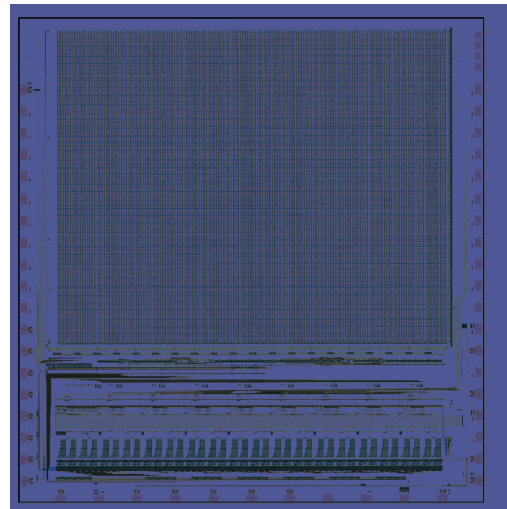
A higher scale of integration reduces costly external components:

- On ROIC non-uniformity compensation reduces cost, power, and size of external components.
- The-on chip heater removes the external TE cooler [or heater].
- The-on chip temperature sensor removes the need for an external sensor for FPA temperature control.

2. ROIC ARCHITECTURE

The ISC9604 is a Silicon Readout Integrated Circuit (ROIC) designed to multiplex a monolithically fabricated 160 X 128 array of uncooled bolometers. The device is unique in that it contains on-chip bias compensation of the bolometers to provide uniform output over a wide operating temperature range and integrated heating element and temperature sensor which combined allow the FPA to operate without thermoelectric cooler stabilization.

A block diagram/schematic of the device, Figure 2, shows the organization of the array and the basic amplification path. The bolometers, which are fabricated on top of the readouts while still in wafer form, are sequentially biased and multiplexed to amplifiers in groups of eight (20 X 128 groups). The detector interface is made by a common gate p-channel MOSFET. The MOSFET biases the detector to a unique programmable potential using on-chip 14 bit DACs to vary the MOSFET gate voltage. The drain current from the input MOSFET is integrated over a sample period (8.3 usec) by a resettable integrator and subsequently sample and held for output multiplexing. The reset integrator amplifies and bandlimits the detector signal. A programmable load current is generated by a series connection of three thermally shunted bolometers connected to the source of an n-channel



**Figure 1 - ISC6904 160x128
Advanced Bolometer Readout**

MOSFET with 14 bit DAC programmable gate voltage. The drain current of the n-channel MOSFET is used to offset the detector current such that only temperature difference induced currents are integrated. Digital coefficients for the bias and offset DACs are multiplexed onto the readout from off-chip memory.

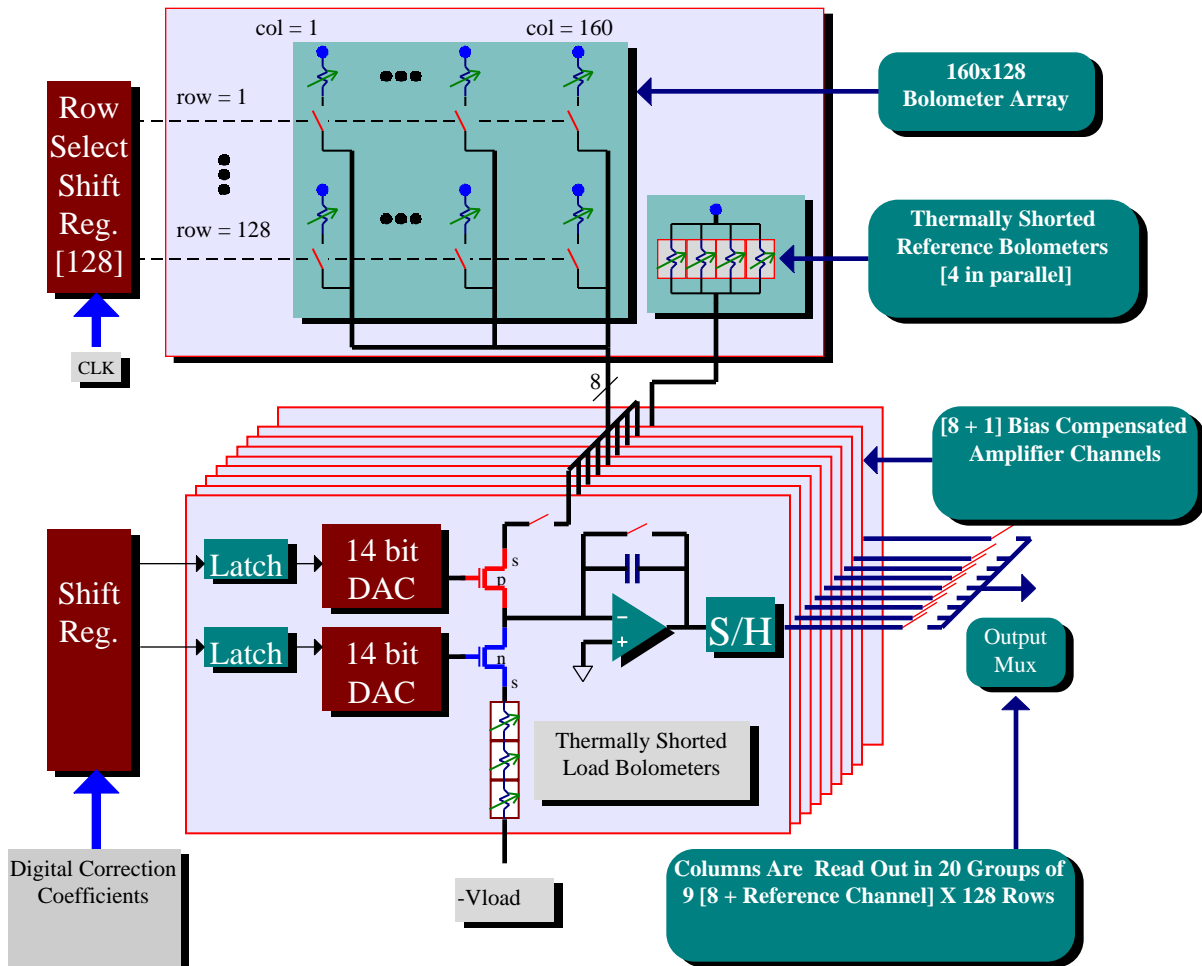


Figure 2. ISC9604 Architecture

Array Performance

The NE_{dT} performance of an FPA resulting from the fabrication of high TCR bolometer on the ISC9604 device can be calculated by:

$$NE_{dT} = NEP / (dM/dT * Fop) \quad \text{where}$$

$$NEP = v_{rms} / (V_{bias} TCR Z_{th}) \quad \text{and}$$

dM/dT change in Exitance/Kelvin, Watts/Kelvin-cm²

Fop Detector-Optics Factor, cm²

v_{rms} rms noise voltage referred to the bolometer, volts

V_{bias} Bias Voltage, volts

TCR Temperature Coefficient of Resistance, %/Kelvin

Z_{th} Thermal Impedance, Kelvin/Watt

By calculating the input referred rms noise voltage and knowing the system optical parameters, the NEdT can be calculated. For the proposed system with $f/2$ optics, $dM/dT \cdot F_{op}$ is $4.97E9$ W/K over the 8 to 13 μ m band taking into account the bolometer emissivity (80%) and optics transmission(90%).

Bolometer Noise Characteristics

The spectral noise of a Vox bolometer is made up of two dominant components, thermal and 1/f noise. The thermal noise of the bolometer resistance, R_{det} , is calculated per a standard Johnson noise source:

$$e_{th}^2 = 4kTR_{det}.$$

While the 1/f noise has been empirically characterized to be dependent upon the bias voltage

$$V_{1/f}^2 (@ 1Hz) = K_{1/f} * V_{bias}^2$$

and rolls off as the square root of frequency. The total noise spectral density generated by the bolometer can be characterized by the summation of the component parts:

$$e_{bol}^2 = V_{1/f}^2/freq + e_{th}^2.$$

Interface Circuit

The equivalent noise voltage, 1/f and thermal, of the interfacing p-channel common gate MOSFET appears in series with the bolometer (and therefore can be added in quadrature to the detector noise):

$$e_{mos}^2 = V_{mos}^2/freq + 8/3kT/gm$$

where gm is the MOSFET transconductance. The 1/f noise of the MOSFET depends upon the fabrication process and the gate area. The ISC9604 input MOS device was designed to contribute very little noise compared to the bolometer contribution.

Offset Load Circuit

In order to provide a temperature compensating offset to the detector current before integration, a current source was formed from three series connected thermally shunted bolometers connected to the source of an n-channel MOSFET. Since the thermally shunted bolometer noise characteristic are the same as the active bolometers, the load circuit will contribute 1/3 of the noise power of the bolometer. The high resistance in the source circuit of the MOSFET essentially eliminates its noise contribution.

Digital to Analog Convertors

The DACs used on the ISC9604 are capacitive ratio devices. Their noise contribution comes from the kTC noise generated during the resetting of the capacitors. This noise is however divided down before application to the MOSFET gate and therefore is calculated to be insignificant:

$$v_{rms} = (kT/C_{dac}) * \text{divide ratio} \quad \text{where}$$

C_{dac} is the total DAC capacitance (10pF) and divide ratio is approximately 0.06 .

Amplifier

The reset integrator noise contribution is small due to the high output impedance of the detector interface MOSFET. In order to input refer the reset integrator noise to the bolometer, the equivalent input noise of the amplifier is divided by the common gate MOSFET drain to source impedance ratio. Since this ratio is very large (>30), the reset integrator and sample and hold contributions are very small.

Reference Channel

A reference channel, made up of the parallel combination of four thermally shunted bolometers four input MOSFETs, amplifiers, loads, etc. is used to provide a signal to be subtracted from the active bolometer signals after multiplexing off of

the FPA. The subtraction of this reference signal removes a great deal of the power supply induced noise and reduces ambient temperature effects. The noise power of this channel is one fourth of an active channel due to its parallel nature.

Noise Computation

A spread sheet of the noise spectral densities as a function of frequency of the various noise components of the ISC9604 FPA was generated using parameters from the ROIC design and known detector characteristics. The noise components were then referred to the chip output by multiplying by the appropriate frequency dependent transfer function. The results of this analysis is displayed in Figure 3. As can be seen the detector noise is the dominant noise component with reference channel and load devices are distant 2nd and 3rd contributors. (The kTC noise terms from the reset integrator, DACs, and Sample and Hold are not shown.)

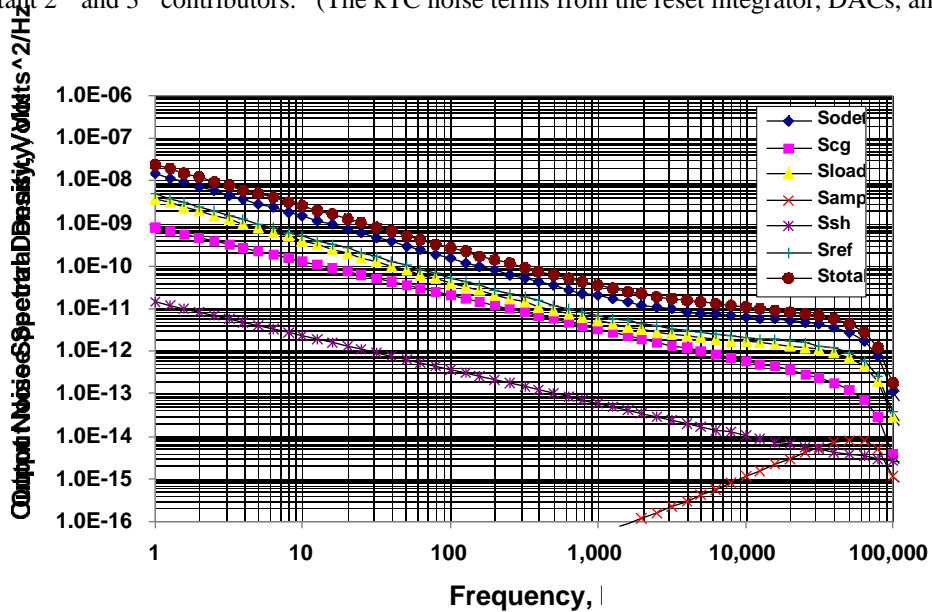


Figure 3. Noise Spectral Density Components of the ISC9604 FPA

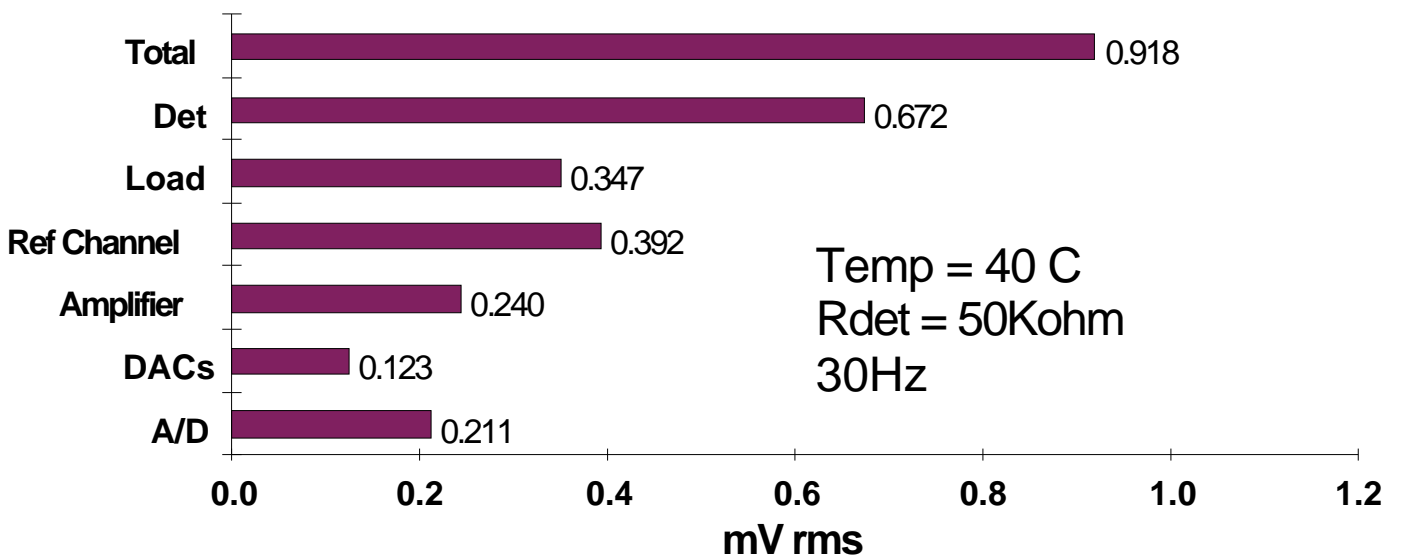


Figure 4 -RMS output noise voltage components

The noise spectrums were integrated over frequency to determine the rms output noise voltage components of the array. This is charted in Figure 4. All of the noise components are presented, including the noise of an external 12 Bit A/D whose dynamic range is matched to the full range output swing. The total output noise is 36% greater than the bolometer's contribution.

The NEdT was calculated by input referring the RMS output noise and applying the NEdT equation initially presented. The calculated NEdT for 4.25V bolometer bias and 2.74% TCR is 72mK [f/1.8].

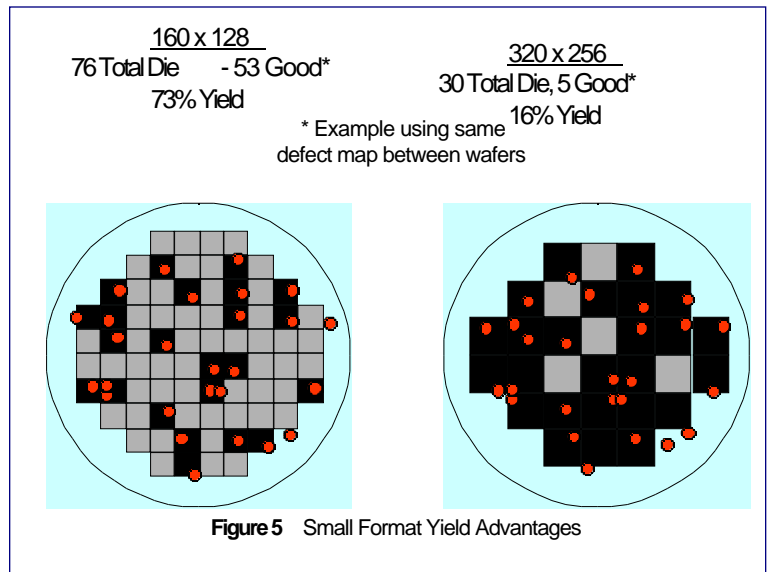
3. ROIC ADVANTAGES

Yield.

By using a 160 x 128 ROIC, four times the die are processed on a wafer compared to an equivalent 320 x 256 ROIC. Given equal processing defects density, it is estimated that FPA yield will be up to eight times that of a 320 x 256 ROIC [see Figure 5.].

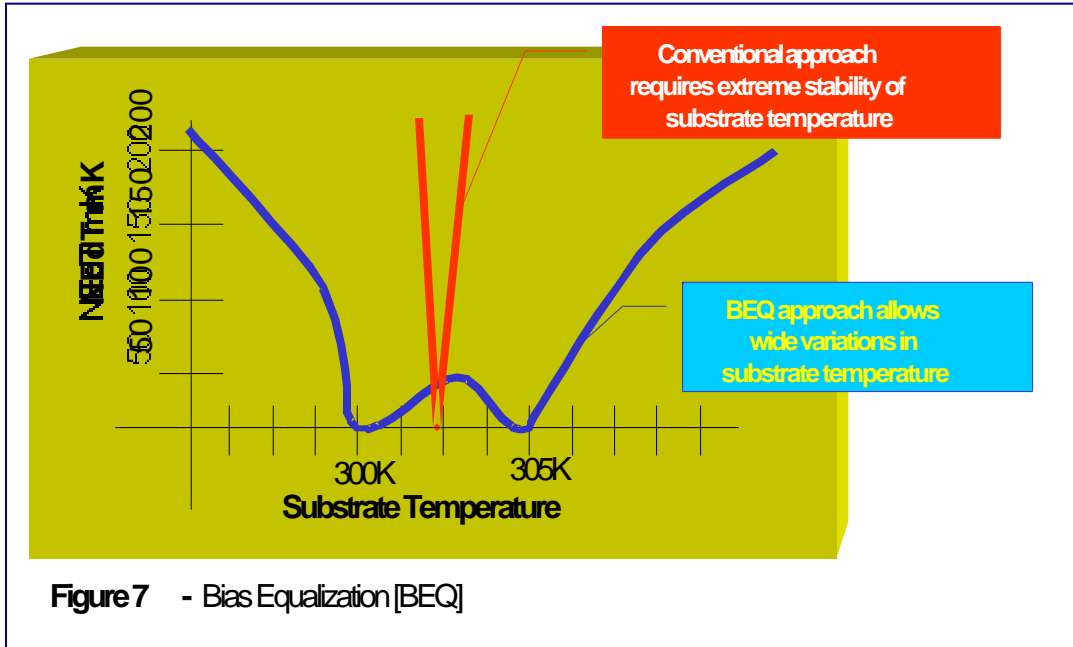
Performance Trade.

By using smoothing in the signal processing chain, low resolution systems used for viewing by humans provide surprisingly good imagery, which is certainly adequate for many applications that are constrained by size, weight, power, and or cost. Figure 6 below compares two cooled InSb images, one taken with a 256 x 256 sensor, and one taken with a 128 x 128 window using the same sensor. The 128 x 128 image has been smoothed. The object in the 128 x 128 image was moved closer so that the object size is the same in both images.



On Chip Correction and Bias Equalization.

The ROIC uses on chip gain and offset normalization for each detector and the reference amplifier. Fourteen bit DACs are used to bias each individual bolometer pixel. By providing this high resolution biasing, the effective response gain of each bolometer can be normalized. Bias Equalization [BEQ] factory calibration takes data for the entire FPA at two different FPA temperatures, at two different black body temperatures. The resultant normalization coefficients are very insensitive to fluctuations in FPA temperature. Figure 7 shows the expected reduced sensitivity to FPA temperature with BEQ.



One set of DACs are used to adjust the bias on each pixel. This technique compensates for variations in:

- Bolometer Resistance
- Bolometer thermal conductivity.
- Bolometer TCR.

The 2nd set of fourteen bit DACs are used to provide an offset term on a pixel by pixel basis. This compensates for variations in:

- Load resistance.
- Amplifier offsets.
- Other system offsets.

Bolometer Protection Circuitry

The normal read time for a bolometer is designed to be 8.3 usec. Applying a bias signal to a bolometer for longer than this time can cause permanent damage to the bolometer. The ISC9604 was designed to allow external fail safe circuits to monitor a clock signal which is returned from the ROIC. If the clock is not present, the external circuits de-assert the frame sync signal, which prevents biasing of any bolometer.

Built In Test.

Three Built In Test modes are supported by the ROIC:

- ROIC test mode.
- Bolometer test mode.
- System test mode.

ROIC test mode.

Initial characterization testing and production testing features are built into the ROIC. Resistive loads simulating bolometers may be switched into the ROIC in a special test mode. This allows independent characterization and production testing of the DACs, amplifiers, and output stages.

Bolometer test mode

To test bolometer processing, the ROIC also supports another test mode where each individual bolometer can be selected and measured.

System test mode.

The third test mode is available at all times, even after camera and systems integration. To use this mode, the ROIC is 'over scanned'. During the over scan time, a set of MOSFETs are switched into the system providing a dummy load for the ROIC signal processing chain. This mode can be very useful during debug and integration of camera systems.

4. EXPECTED AND MEASURED PERFORMANCE

Summary

The ISC9604 characterization testing showed excellent performance, closely matching the design goals and simulations results. Five ISC9604 ROICs were tested using the ISC Characterization Test Station. All die showed results consistent with the data presented.

General Operations

Power Disipation

The design value for ISC9604 power was 36 mW. The measured value was 33mW.

Video Output Rise Time.

The settling time was measured to be less than 100nS, which is consistent with the output rate of 3MHz.

On Chip Heater

The resistance of the on-chip heater was measured at 300 ohms, vs. a design goal of 250 ohms.

Bolometer Protection Circuitry

Holding the frame sync signal low was observed to prevent biasing of the bolometers. [see the previous description of this feature]

DAC Testing Goals

Exercising the DACs and observing their effects on the 9 group amplifiers was the primary goal of the ISC9604 Characterization Testing. Each DAC has 14 bits, which is comprised of two 7 bit DACs that are summed. The overall goal of the testing was to show that each individual DAC was monotonic, and that the full scale range of the [least significant] LSB DAC was larger than the smallest single step of the [most significant]LSB DAC.

DAC Testing Results

As can be seen from the data provided, all DACs tested were monotonic. The overlap of the LSB and MSB DACs was also sufficient to ensure full-scale operation. Data was taken on both the reference channel, and the 8 'group' channels. Reference channel data was representative of DAC behavior for all DACs, and is reported herein.

The following characterization data samples describe the format and content of the data included in the appendix.

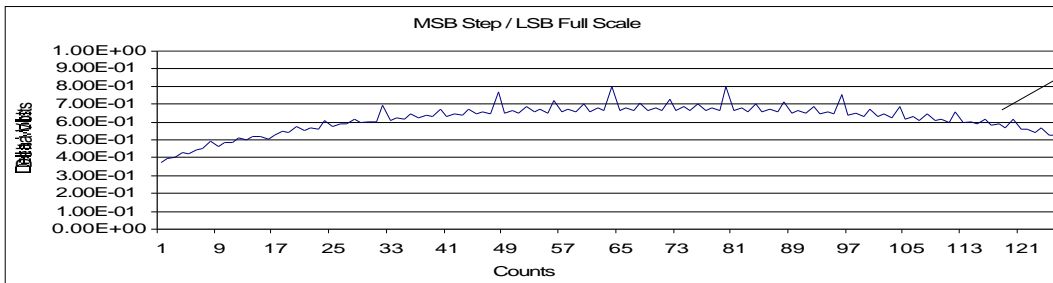
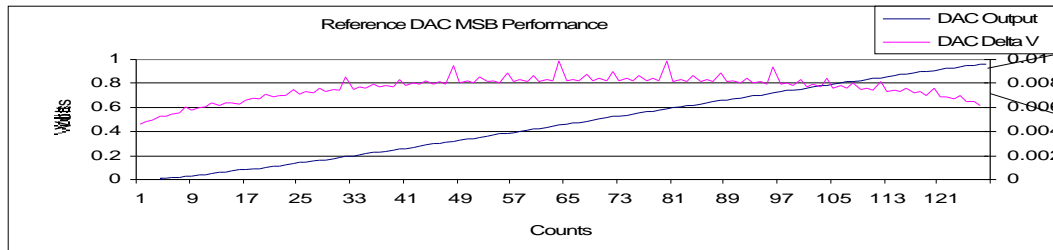
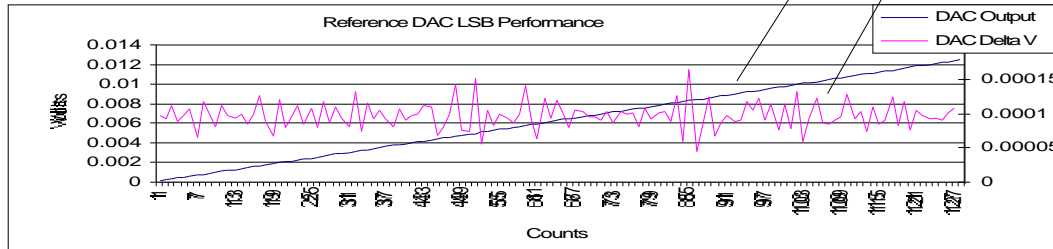
Noise

The output amplifier noise was consistent with the noise predictions in Figure 4.

DAC Mononicity Data Legend

The subheadings under this section refer to the callouts in this sample data.

	LSB	MSB
FullScale [V]	1.23E-02	9.70E-01
AverageLSB [V]	9.72E-05	7.64E-03
MinimumStep [V]	4.44E-05	4.66E-03
MaximumStep [V]	1.64E-04	9.88E-03



Callout 1: Statistics

This section shows the Mean, Sigma, Maximum, and Minimum single DAC count values for both the LSB and the MSB of the DAC tested.

Callout 2: DAC. LSB Voltage Output vs. DAC Count

This line on the indicated chart shows the raw output voltage vs. the DAC counts

Callout 3: DAC LSB Volts per Count

This line is the derivative of the Voltage Output vs. DAC Count line. If no derivatives are less than zero, the test of this DAC is considered a success.

Callout 4: DAC. MSB Voltage Output vs. DAC Count

This line on the indicated chart shows the raw output voltage vs. the DAC counts

Callout 5: DAC MSB Volts per Count

This line is the derivative of the Voltage Output vs. DAC Count line. If no derivatives are less than zero, the test of this DAC is considered a success.

Callout 6: DAC MSB Step ratio to DAC LSB Full Scale

This line shows the ratio of the DAC MSB single count size to the DAC LSB Full Scale voltage. If this ratio were to exceed one, the overall DAC [made up of the two 7 bit DACs] would have large jumps in voltage. This test is considered a success if the ratio is less than one over the entire DAC range.

5. CONCLUSIONS

A new approach for a bolometer ROIC has been designed and tested. This novel approach can significantly reduce the system design complexities and improve the performance of uncooled bolometer systems. While approach used in this small format array is scalable to larger formats, the selected 160 x 128 format provides several advantages that enable further system level reductions in size, weight, power, and cost.